REMARKS

With claims 1-47 previously pending, with this response, claims 43-47 that were withdrawn under a restriction requirement have been cancelled. Further claims 4, 10 and 19 have been cancelled and claim 1 has been amended as indicated in detail below.

Drawing Objections

The Office Action indicates that the drawings must show every feature of the invention specified in the claims. The Office Action continues stating that the features in claims 9-10, 23, 33 and 37 must be shown or the feature(s) canceled from the claims.

The features in claims 9-10, 23, 33 and 37 are believed shown in the drawings without further modification. In particular, regarding claim 9, paragraph [0032] of Applicants' specification indicates that a row segment shown in Fig. 3 can be formed as a tile and replicated any number of times. Claim 10 has been cancelled. Regarding claim 23, 33 and 37, paragraphs 19 and 63 of Applicants' specification refer to Fig. 10 and indicate the memory is a configuration memory for a programmable logic device as claimed. Accordingly, the drawings are believed unobjectionable without amendment.

Claim Objections

The Office Action indicates that withdrawn claims 43-47 should be cancelled in response to this Office Action. Accordingly, this response cancels claims 43-47.

Section 112, First Paragraph Rejection

Claims 1-42 stand rejected under 35 U.S.C. § 112, first paragraph, as non-enabling.

Initially, the Office Action states that it is not understood how the logic 800 in Fig. 8 can be one embodiment of logic 500 of Fig. 5 as described in lines 1-2 of paragraph [0057], since Fig. 5 does not show any logic 500; WR-E, POR, PCH, and

PDCH as shown in Fig. 8; PCH; WR-EN, POR, PDCH, POR and PDCH as shown in Fig. 9.

In response, applicants have amended paragraph [0057] to correctly refer to the "logic 510" instead of "logic 500" to comply with Fig. 5A. This was due to a clerical error and no new matter has been added.

The Office Action next states that it is not understood what is "To next row" as shown in Figs. 5B, 12 and 13B and as recited in claims 38 and 40-42.

In response, Applicants believe the Figs. 2, 3 and 5 in combination with their description adequately indicate what "To next row" means in Figs. 5B, 12 and 13B. As indicated by the figure descriptions, Fig. 3 shows details of one embodiment of a row of the array of Fig. 2. In Fig. 2, the RD/WR signals are provided from the control circuit 230 to the adjacent DL Drivers 214(1) and 214(2). Fig. 3 shows that the RD/WR signals pass through the DL Driver 214(1), on their way to adjacent DL Driver 214(2) in compliance with Fig. 2. Fig. 5 shows one embodiment of the row of Fig. 3. In particular, Fig. 5B shows that the RD/WR signals from the controller 230 passes through the DL Driver 214(1), complying with Fig. 2, on their way to DL Driver 214(2). Accordingly, the RD/WR signals are believed adequately described as being passed from the controller 230 through a first DL Driver then "to the next row" to a second DL Driver and so forth.

The Office Action continues stating that it is not understood how data propagation occurs only in a first direction from the second row segment to the first row segment during a read operation and only in a second direction from the first row segment to the second row segment during a write operation as recited in claims 1-42 since there are a plurality of row segments 212. The Office Action asks how the data is propagated in the remaining row segments.

In response, Applicants' specification explains the propagation process, particularly beginning in paragraph [0027], and proceeding with detail as more detailed circuitry is described. As indicated beginning in [0027], data is propagated in a first direction for writing from the control circuit 230 to the appropriate segment 212(n), as controlled by DL drivers 214(n) and in a second direction for reading from an appropriate segment 212(n) back into the control circuit 230. DL Drivers 214(n)

separate the memory segments 212(n) as shown in Fig. 2, and control data flow. Fig. 5B shows how DL Drivers include logic (such as 537, or 541) to enable data flow on data lines DL(1), DL(2) in one direction only depending on whether WR or RD is asserted. Thus in response to the Office Action, data is propagated from a memory cell in one segment 212(n) through adjacent segments 212(n) and DL drivers 214(n) to the control circuit 230 during read, and from the control circuit 230 through adjacent cells 212(n) to an appropriate memory cell during write.

Based on the above remarks, Applicants maintain that all claims are now believed enabling under 35 U.S.C. § 112, first paragraph.

Section 112, Second Paragraph Rejection

Claims 4, 19, 25, 38 and 40-42 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claims 4 and 19 have been cancelled rendering this rejection moot with respect to those claims.

Regarding claim 25, the Office Action states that it is not clear what type of combination of a control signal and a data on the dataline segment in the second adjacent row segment occurs since there are a plurality of row segments and dataline drivers.

In response, Applicants refer to the specific circuitry of Fig. 5B that is believed to clearly show both control signals and dataline signals. As shown in Fig. 5B, a dataline driver 214(1) receives control signals (RD/WR) as well as data from dataline segments (DL(1), DL(2)) from adjacent segments. The combination of control and data signals allows data to travel from a memory cell of a segment toward control circuit 230 during read, and from control circuit 230 to a segment during write as described above with respect to paragraph [0027].

Regarding claims 38 and 40-42, the Office Action states that it is unclear what a next row really is since there are a plurality of row segments cited.

In response, applicants point out that the language of claim 38 is believed to include language to adequately indicate what "next row" means. Claim 38 claims a plurality of row segments "each having a dataline segment connected to a dataline

segment in an adjacent row segment by a corresponding dataline driver." Claim 38 continues to claim "configuring each dataline driver ... in a first direction from a previous row segment to a next row segment...." Thus, with the dataline driver claimed to have adjacent row segments, one will be previous and the other will be next. A similar explanation is appropriate for claims 40-42 that depend on claim 38.

Accordingly, claims 25, 38 and 40-42 are now all believed allowable as definite under 35 U.S.C. 112, second paragraph.

Section 103 Rejection

Claims 1-42 stand rejected as being unpatentable over Iminki et al. (U.S. Patent No. 5,847,890, hereinafter "Iminki".) The Office Action states that Iminki discloses in Fig. 2 a memory device 202 comprising: a plurality of row segments 210-1 to 210-m; and a bidirectional gate 204 for driving the write data path and a read data path in response to write/read control signal (see lines 11-12, col. 5) obviously considered connected between row segments through respective sense amplifiers 214-1 to 214-m and analog-to-digital A/D circuit 216-1 to 216-m. The Office Action continues indicating that as understood with the Section 112 Rejections pending, all the remaining features as recited in claims 1-42 are also rendered obvious under 35 U.S.C. § 104 over Fig. 2 of Iminki. Based on the following remarks, this rejection is respectfully traversed.

Initially, independent claim 1 has been amended to claim a control circuit providing read and write control signals to the dataline driver, and that the dataline driver is connected between the first and dataline segments to enable propagation of data either toward the control circuit during a read, or away from the control circuit during a write operation. Such a control circuit 230 and driver 214(n) is shown throughout Applicants' figures and described in the specification.

Iminki's bidirectional gate 204 does not disclose both the dataline driver and control circuit claimed in claim 1. Particularly, with the dataline driver circuit receiving read and write control signals from the control circuit and then operating to propagate data signals either toward or away from the control circuit. Claim 1 is, thus, believed allowable as non-obvious over Iminki.

Claims 2-3, 5-9, 11-18 and 20-24 are believed allowable as non-obvious over Iminki based at least on their dependency on claim 1. These claims are further believed allowable based on additional features claimed not shown by Iminki. For example, claim 5 includes AND and OR gates of the dataline driver that enable propagation of data in only one direction. Iminki is not believed to teach or disclose these specific features.

Regarding independent claims 25, 34 and 38, these claims all include multiple dataline drivers provided in-between row segments in contrast with Iminki. Iminki's bi-directional gate 204 only provides one device for driving row lines. The multiple dataline drivers claimed by claims 25, 34 and 38 further control data to travel in one direction in particular row segments, in contrast with Iminki. Accordingly, claims 25, 34 and 38 are believed allowable as non-obvious over Iminki.

Claims 26-33, 35-37 and 39-42 are believed allowable as non-obvious over Iminki based at least on their dependency on respective ones of claims 25, 34 and 38.

Conclusion

All claims should now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, Applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

Kim Kanzaki, Ph.D.
Attorney for Applicants
Reg. No. 37,652

I hereby certify that this correspondence is being deposited with the United States Postal Service as ***first class mail*** *in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on January 31, 2006.*

Pat Tompkins
Name

Signature